EXHIBIT K

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.; MICRON SEMICONDUCTOR PRODUCTS, INC.; and MICRON TECHNOLOGY TEXAS LLC,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case No. IPR2022-00236
U.S. Patent No. 9,824,035

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 9,824,035

331–334, which supplies data DQ to input or output terminals, 341 and 342, to certain memory chips 200. Ex. 1003, ¶ 111; Ex. 1005, [0094], [0097]. This interpretation is consistent with how the '035 patent describes "*enabling a data path*." *See* Ex. 1001, 5:43–45, 12:10–20, 18:10–15. Such a person would have recognized that these terminals are connected to the L1 and L2 lines that connect to memory chips 200. Ex. 1003, ¶ 111; *see* Ex. 1005, Fig. 1. Accordingly, data register buffer 300 includes "*logic configured to enabl*[*e*]…*data paths*" in "*respon*[*se*] *to the module control signals*." Ex. 1003, ¶ 111.

As Dr. Alpert explains, a POSITA would have recognized that this data register control circuit 320 (the claimed "*logic*") also includes the read leveling and write leveling circuits 322 and 323. Ex. 1003, ¶ 112. Such a person would have recognized that both read and write leveling circuitries compensate for propagation delays caused by some memory chips being placed farther away from their respective data register buffers. *Id.*; Ex. 1005, [0146].

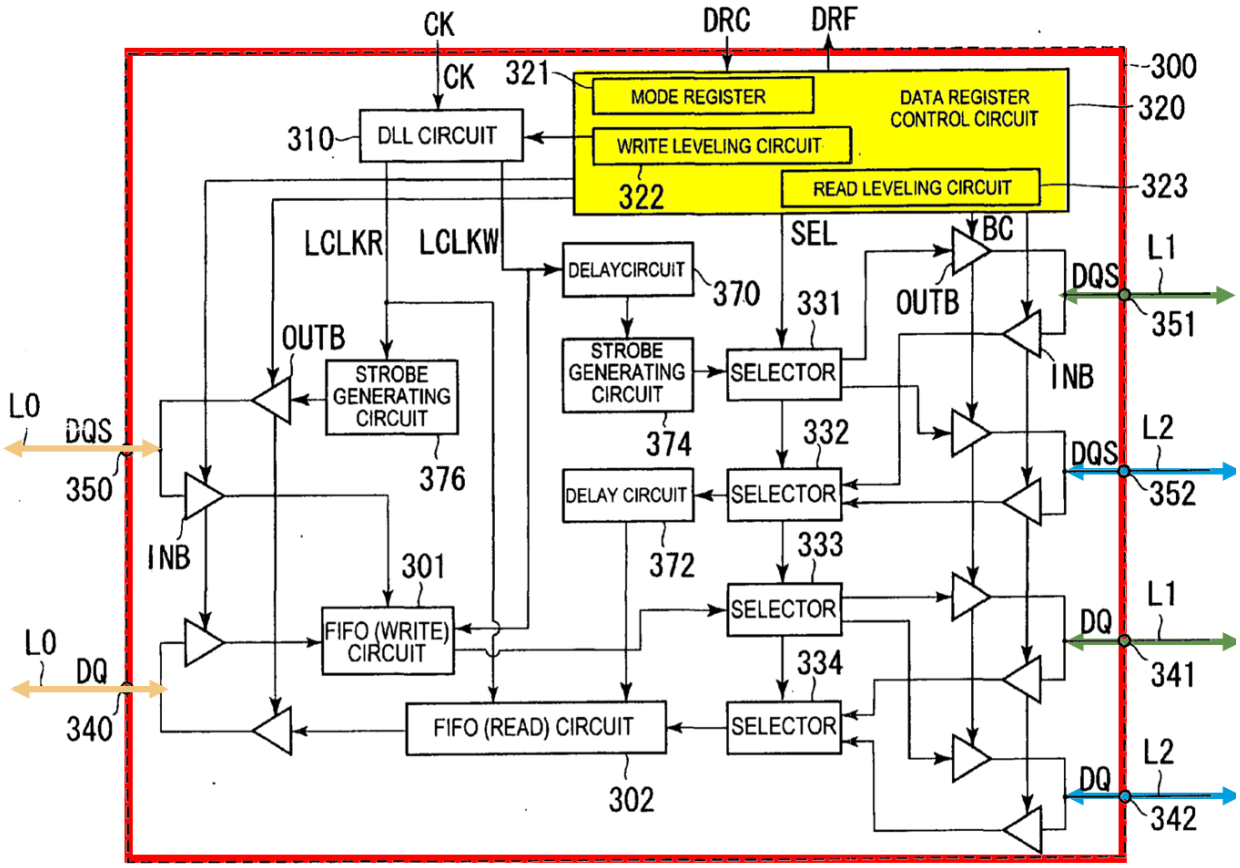
j. Obtaining Timing Information

Claim 1 recites "*logic* [*that*] *is further configured to obtain timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation to control timing of the respective data and strobe signals on the data paths in accordance with the timing information*." As explained below, Osanai discloses the claimed "*logic*," but

does not expressly disclose that the timing information is obtained "*during a second memory operation prior to the first memory operation*." Tokuhiro, however, discloses a technique that obtains timing information "*during a second memory operation prior to the first memory operation*." It would have been obvious to incorporate Tokuhiro's technique in Osanai's "*logic*," as further explained below.

i. Osanai discloses "*logic* [*that*] *is further configured to obtain timing information based on one or more signals received by the each respective buffer circuit*" used "*to control timing of the respective data and strobe signal on the data paths in accordance with the timing information.*"

Osanai discloses both read and write leveling techniques, which are performed by circuitry 322 and 323 located in the data register control circuit 320. *Id.* at [0096]; *see also id.*, [0146]–[0164], Figs. 14A–17. These techniques make timing adjustments so that signals between "the memory chips 200 and the data register buffer 300" are sent at the appropriate time. Ex. 1005, [0110]; *see also id.*, [0096], [0146]. Figure 5 illustrates that the data register buffer 300 includes read and write leveling circuits:



Ex. 1005, Fig. 5; Ex. 1003, ¶¶ 115–116. To make these adjustments, the read and write leveling circuitry use the module clock (CK) signal ("*one or more signals received by the each respective buffer circuit*") sent from the command/address/control register buffer 400. *See* Ex. 1005, Fig. 5, CK, Fig. 7, Clock-Post. Based on this clock signal, a "timing adjustment"—an added time delay—is used to create DQ-Post and DQS-Post. Ex. 1005, [0110]; *see id.*, [0149]–[0157]; Ex. 1003, ¶¶ 117. In doing so, the leveling circuitry "adjust[s] a write timing

or a read timing in consideration of a propagation time of a signal." Ex. 1005, [0146], [0149]–[0157]; Ex. 1003, ¶ 117.

Thus, Osanai discloses "*obtaining timing information*" for both read and write leveling techniques. Ex. 1003, ¶ 118. And Osanai discloses how this timing information is based on a module clock signal ("*one or more signals received by the each respective buffer circuit*"). *Id.* But Osanai does not explicitly disclose that the timing information is obtained "*during a second memory operation prior to the first memory operation*." As explained below, however, Tokuhiro renders this feature obvious.

ii. Tokuhiro discloses a technique to obtain timing information "*during a second memory operation prior to the first memory operation*."

Like Osanai, Tokuhiro discloses read and write leveling techniques. Tokuhiro explains that such leveling techniques are necessary to compensate for different propagation delays. Ex. 1006, 1:63–2:9; Ex. 1003, ¶ 120. Specifically, Tokuhiro states that propagation delays differ because memory units have different wiring lengths. *Id*. To compensate for these different delays, Tokuhiro's technique "employ[s] the write leveling function." *Id.*, 2:46–49. Tokuhiro recognized that the "delay [determined from the write leveling function] may affect [] reading data from the SDRAM 92," as well. *Id.* 3:9–12.

Consequently, Tokuhiro teaches a delay unit that obtains a first delay time from a write operation ("*during a second memory operation*") to use in its calculation of a second delay time ("*obtaining timing information*") used for a read operation ("*the first memory operation*"). *Id*. 3:16–26; Ex. 1003, ¶121. For example, Tokuhiro discloses calculating a second delay time for the read operation based on the first delay time determined by the write level operation:

> In other words, the second delay time Dt2 for the data signal DQ input from the SDRAM can be calculated by using the first delay time Dt1 that has been set in the write leveling. Accordingly, in the second delay time control unit 24, the second delay time Dt2-x corresponding to one SDRAM-x is set by using the above-mentioned formula (3-5) so that the sum of the first delay time Dt1-x and the second delay time Dt2-x both corresponding to the relevant SDRAM-x is equal to a preset value.

Id., at 16:1–28, Abstract. Because Tokuhiro uses "*timing information*" determined during the write operation for a subsequent read operation, it follows that the write operation necessarily occurred before the read operation. Ex. 1003, ¶ 121. Therefore, Tokuhiro discloses a technique that obtains timing information "*during a second memory operation prior to the first memory operation*." *Id.*

The challenged claims encompass Tokuhiro's technique which mirrors the '035 patent's description of how the timing information is obtained. Ex. 1003, ¶ 122.

Specifically, the '035 patent explains that timing information is determined during a write operation and used to determine a delay in a subsequent read operation:

> [E]ach buffer circuit includes signal alignment circuits that determine, *during a write operation*, a time interval between a time when one or more module control signals are received from the module control circuit and a time when a strobe or data signal is received from the memory controller. *This time interval is used during a subsequent read operation* to time transmission of read data to the memory controller, such that the read data arrives at the memory controller within a time limit in accordance with a read latency parameter associated with the memory system.

Ex. 1001, 4:7–17 (emphasis added); *see also id.*, Claim 2. As explained above, Tokuhiro also discloses that timing information determined during a write operation is used in determining a delay for subsequent read operations. Ex. 1006, 3:16–26, 16:1–28. Consequently, Tokuhiro discloses the same technique that is described by the '035 patent—but years earlier.

iii. It would have been obvious to use Tokuhiro's technique in Osanai's buffer leveling circuitries.

Osanai and Tokuhiro are analogous art to the '035 patent. Ex. 1003, ¶ 124. First, they are directed toward the same field of endeavor—namely, memory modules. Ex. 1001, 1:34–36; Ex. 1005, [0001], Ex. 1006, 1:15–20. Alternatively,

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Respectfully submitted,

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